Amend claim 6 as follows:

--6. (amended) A semiconductor memory device having a plurality of memory blocks, each block including a plurality of memory banks, wherein a target memory cell in the memory blocks is accessed according to an input bank address, row address, and column address, the semiconductor memory device comprising:

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a row decoding section for decoding the row address so as to generate a row selecting signal;

a column pre-decoding section for pre-decoding the column address so as to generate a column pre-decoded signal; and

a column decoding section, provided in an area of the memory block where a sense amplifier for sensing the memory cell is provided, for performing the main decoding operation of the column address based on the column pre-decoded signal, and selecting the column on the memory block designated by the column address,

wherein the column decoding section generates a column selecting signal by performing the main decoding operation of the column address, and

word lines driven by the row selecting signal and column selecting signal lines for outputting the column selecting signal are arranged parallel to each other, so as to

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supply these signals to the memory block of the target memory cell and to access the memory cell.--

Amend claim 8 as follows:

--8. (amended) A semiconductor memory device having a plurality of memory blocks, each block including a plurality of memory banks, comprising:

a connecting portion, provided [on] above each memory cell in the memory blocks, for connecting metallic wiring layers.--

Add the following new claims:

~~14~~ 10. A semiconductor memory device as claimed in claim 1, wherein the semiconductor memory device is a DRAM.

~~15~~ 11. A semiconductor memory device as claimed in claim 6, wherein the semiconductor memory device is a DRAM.

--16. A semiconductor memory device as claimed in claim 8, wherein the semiconductor memory device is a DRAM.

--17. A semiconductor memory device as claimed in claim 10, wherein the semiconductor memory device is a DRAM.

~~18~~ 12. A semiconductor memory device as claimed in claim ~~11~~ 8, wherein the semiconductor memory device is a DRAM.

--19. A semiconductor memory device as claimed in claim 13, wherein the semiconductor memory device is a DRAM.

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~~20~~. A semiconductor memory device as claimed in claim 1, further comprising:

a connecting portion, provided above each memory cell in the memory blocks, for connecting metallic wiring layers.

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--~~21~~. A semiconductor memory device as claimed in claim 13
~~20~~, wherein the connecting portion is provided for connecting each column selecting signal line to a sense amplifier for sensing the memory cell.

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~~22~~. A semiconductor memory device as claimed in claim 1, wherein:

the target memory cell in the memory blocks is accessed via input/output lines; and

the column selecting signal lines and the input/output lines are arranged perpendicular to each other.--

Please charge the fee of $36 for the addition of two claims of any type in excess of the 20 originally paid for to Deposit Account No. 25-0120.

R E M A R K S

The specification and drawings have been amended to make editorial changes therein, bearing in mind the criticisms in the Official Action, to place the application in condition for allowance at the time of the next Official Action.

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